Having thus described the invention, it is now claimed:

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1. A method of operating a processor to repeatedly execute at least one associated instruction, comprising:

loading a register with a count value indicative of the number of times the associated instruction is to be executed;

fetching and executing a REPEAT instruction indicating the at least one associated instruction to be repeatedly executed;

fetching the at least one associated instruction; and

executing the at least one associated instruction for as many times as indicated by the count value.

2. A method of operating a processor to repeatedly execute one or more instructions, comprising:

fetching a REPEAT instruction;

executing a REPEAT instruction, wherein execution of the REPEAT instruction stores in a register a count value indicative of the number of times one or more associated instructions are be executed;

fetching the one or more associated instructions; and

executing the associated instruction for as many times as indicated by the count value.

3. A method of operating a processor to repeatedly execute one or more instructions, comprising:

loading a register with a count value indicative of the number of times one or more associated instructions are to be executed;

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fetching and executing a REPEAT instruction indicating the one or more associated instructions that are to be repeatedly executed;

incrementing a program counter;

fetching the one or more associated instructions; and

executing the one or more associated instruction for as many times as indicated by a count value stored in a count register.

4. A method of operating a processor according to claim 3, wherein said count value is stored in said count register before execution of said REPEAT instruction.

5. A method of operating a processor according to claim 3, wherein said REPEAT instruction includes the count value that is stored in said count register, wherein execution of the REPEAT instruction stores the count value in said count register.

6. A method of operating a processor according to claim 3, wherein said method further comprises:

incrementing the program counter after the one or more associated instructions have been executed for as many times as indicated by the count value.

7. A method according to claim 3, wherein method further comprises:

decrementing said count value stored in said register each time said one or more associated instructions are executed; and

determining whether said count value is less than or equal to zero.

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8. A processor for repeatedly execute at least one associated instruction, said processor comprising:

load means for loading a register with a count value indicative of the number of times the associated instruction is to be executed;

first fetch means for a REPEAT instruction indicating the at least one associated instruction to be repeatedly executed;

first execute means for executing the REPEAT instruction indicating the at least one associated instruction to be repeatedly executed;

second fetch means for fetching the at least one associated instruction; and

first execute means for executing the at least one associated instruction for as many times as indicated by the count value.

9. A processor for repeatedly executing one or more instructions, comprising:

first fetch means for fetching a REPEAT instruction;

first execute means for executing a REPEAT instruction, wherein execution of the REPEAT instruction stores in a register a count value indicative of the number of times one or more associated instructions are be executed;

second fetch means for fetching the one or more associated instructions; and

second execute means for executing the associated instruction for as many times as indicated by the count value.

10. A processor for repeatedly executing one or more instructions, comprising:

load means for loading a register with a count value indicative of the number of times one or more associated instructions are to be executed;

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first fetch means for fetching a REPEAT instruction indicating the one or more associated instructions that are to be repeatedly executed;

first execute means for executing the REPEAT instruction indicating the one or more associated instructions that are to be repeatedly executed;

means for incrementing a program counter;

second fetch means for fetching the one or more associated instructions; and

second execute means for executing the one or more associated instruction for as many times as indicated by a count value stored in a count register.

11. A processor according to claim 10, wherein said count value is stored in said count register before execution of said REPEAT instruction.

12. A processor according to claim 10, wherein said REPEAT instruction includes the count value that is stored in said count register, wherein execution of the REPEAT instruction stores the count value in said count register.

13. A processor according to claim 10, wherein said processor further comprises:

means for incrementing the program counter after the one or more associated instructions have been executed for as many times as indicated by the count value.

14. A processor according to claim 10, wherein processor further comprises:

means for decrementing said count value stored in said register each time said one or more associated instructions are executed; and

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means for determining whether said count value is less than or equal to zero.

15. A processor for repeatedly executing one or more processor instructions, said processor comprising:

a memory address register associated with a main memory;

a memory data register associated with the main memory;

a memory control for generating memory control signals;

a program counter for storing a memory address location of the main memory where an instruction is to be fetched;

an instruction register for storing an instruction that is to be executed;

at least one general purpose register;

decode and execute control logic for decoding and executing an instruction stored in the instruction register; and

a state machine for controlling the fetching and repeated execution of one or more associated instructions.

16. A processor according to claim 15, wherein said processor further comprises an instruction buffer for storing the one or more associated instructions.

17. A processor according to claim 15, wherein said general purpose register includes a first register for storing a count value indicative of the number of times the one or more associated instructions are to be repeatedly executed.

18. A processor according to claim 17, wherein said state machine generates signals for decrementing the count value stored in the first register.

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19. A processor according to claim 17, wherein said state machine generates a signal for executing an instruction stored in said instruction register.

20. A processor according to claim 17, wherein said state machine generate a signal for incrementing said program counter.